WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on an insulating substrate and including a gate line and a gate electrode connected to the gate line;

a storage capacitor wire formed on the insulating substrate and having a storage capacitor electrode line and a storage electrode connected to the storage capacitor electrode line and located at an edge of a pixel area;

a gate insulating film covering the gate wire and the storage capacitor wire;

a semiconductor layer formed on the gate insulating film;

a data wire formed on the gate insulating film or the semiconductor layer and including a data line intersecting the gate line to define the pixel area, a source electrode connected to the data line and located on the semiconductor layer, a drain electrode formed on the semiconductor layer and located opposite the source electrode with respect to the gate electrode, and a first storage capacitor conductor overlapping the storage electrode via the gate insulating film to form a storage capacitor; and

a pixel electrode electrically connected to the drain electrode and the first storage capacitor conductor.

2. The thin film transistor array panel of claim 1, wherein the drain electrode is connected to the first storage capacitor conductor.

3. The thin film transistor array panel of claim 1, further comprising a second storage capacitor conductor overlapping a previous gate line to form a storage capacitor at an edge of the pixel area.

4. The thin film transistor array panel of claim 1, further comprising a protective layer formed between the pixel electrode and the drain electrode and the first storage capacitor conductor.

5. The thin film transistor array panel of claim 1, wherein the semiconductor layer except for a channel area between the source electrode and the drain electrode has substantially the same pattern as the data wire.

6. The thin film transistor array panel of claim 1, further comprising an ohmic contact pattern formed between the semiconductor layer and the data line and has the same pattern as the data line.

7. A liquid crystal display comprising the thin film transistor array panel of claim 1.

8. The liquid crystal display of claim 7, further comprising a black matrix having an aperture in the pixel area, at least one portion of the black matrix overlapping the first storage capacitor conductor.